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(71) Applicant *(for all designated States except US)*: **INTERNATIONAL BUSINESS MACHINES CORPORATION** [US/US]; New Orchard Road, Armonk, NJ 10504 (US).

(72) Inventors; and

(75) Inventors/Applicants *(for US only)*: **ARTHANARI, Geetha** [IN/US]; 38 Thasha Lane, I-4, Essex Junction, VT 05452 (US). **CARRIG, Keith, M.** [US/US]; 74 South Street, Unit E, Essex Junction, VT 05452 (US). **LASHER, Mark, R.** [US/US]; 146 Lindale Drive, Colchester, VT 05446 (US). **MENARD, Daniel, R.** [US/US]; 9 Acton Street, Arlington, MA 02476 (US).

(74) Agent: **NEFF, Daryl, K.**; International Business Machines Corporation, Dept. 18G/Bldg. 300-482, 2070 Route 52, Hopewell Junction, NY 12533 (US).

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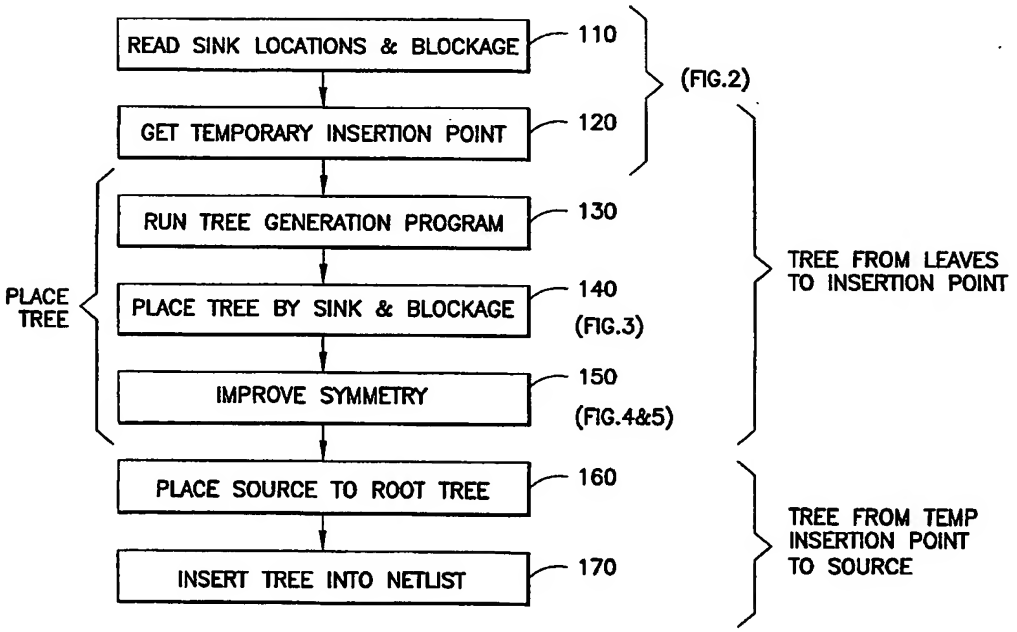
(54) Title: ASIC CLOCK FLOOR PLANNING METHOD AND STRUCTURE



(57) Abstract: A method of designing a clock tree in an integrated circuit combines steps of making a list of all clock sinks (110); positioning a temporary reference insertion point (TIP) (120); grouping the sinks together with structured clock buffers (SCBs) in a set of levels (140); and moving the SCBs to improve symmetry of the tree (150). The SCBs may be of several sizes and may be positioned horizontally (42) or vertically (45) and moved within limits (46) to permit the program to calculate a complete tree.

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